REMARKS

Claims 1-11, 13-18, 20-21, 23-52, and 57-59 were previously pending in this patent application. Claims 1-11, 13-18, 20-21, 23-52, and 57-59 stand rejected. Herein, Claim 50 has been canceled. Further, Claims 1, 11, 17, 18, 35, 37, 42, 44, 51, 52, and 58 have been amended. Support for the amendments is found on page 47, lines 12-21, of the Specification. Accordingly, after this Amendment and Response After Final Action, Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

35 U.S.C. Section 102(a) and (b) Rejections

Claim 50 stands rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Furtek et al., U.S. Patent No. 5,894,565 (hereafter Furtek). These rejections are moot since Claim 50 has been canceled.

35 U.S.C. Section 103(a) Rejections

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Furtek et al., U.S. Patent No. 5,894,565 (hereafter Furtek). These rejections are respectfully traversed.

Independent Claim 1 recites (as amended):

A microcontroller circuit comprising:
a bus;
a microprocessor coupled to said bus;
a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and
a plurality of functionalities coupled to said bus, wherein said non-volatile memory functions to program said functionalities and wherein said plurality of functionalities comprise:
an interconnect wherein said interconnect is dynamically configurable and programmable;
an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and
a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***. (emphasis added)

It is respectfully asserted that the combination of Insenser and Furtek does not teach, suggest, or motivate the present invention as recited in Independent Claim 1. In particular, the Independent Claim 1 recites the limitation, "said dynamically configurable and programmable digital functional block ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***," (emphasis added). In contrast, Insenser states that the FIPSOC architecture is reconfigurable by issuing a microprocessor command, and the reconfiguration time would be that of a microprocessor write cycle. [Insenser; Col. 5, lines 1-9]. However, Insenser fails to teach, suggest, or motivate that a dynamically configurable and programmable digital functional block is

configurable with a single register write operation, as in the invention of Independent Claim 1.

Further, Furtek shows logic cells having two 8x1 static RAMs whose content may be dynamically changed to reconfigure the logic functions carried out by the logic cells. [Furtek, Col. 9, lines 35-43]. The reconfiguration involves providing write access to the SRAMs using a DATA_In line, providing address inputs a0-a2, and providing a write enable signal WE from write enable circuitry to the SRAMs. [Furtek, Col. 10, lines 4-34]. However, Furtek fails to teach, suggest, or motivate that a dynamically configurable and programmable digital functional block is configurable with a single register write operation, as in the invention of Independent Claim 1.

As described above, the combination of Insenser and Furtek does not teach, suggest, or motivate the cited claim limitation of Independent Claim 1. Therefore, it is respectfully submitted that Independent Claim 1 is patentable over the combination of Insenser and Furtek and is in condition for allowance.

Dependent Claims 2-10 are dependent on allowable Independent Claim 1, which is allowable over the combination of Insenser and Furtek. Hence, it is respectfully submitted that Dependent Claims 2-10 are patentable over the combination of Insenser and Furtek for the reasons discussed above.

With respect to Independent Claims 11, 17, 35, 37, 42, 51, and 52, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 recite similar limitations as in Independent Claim 1. In particular, Independent Claims 11, 17, 35, 37, 42, 51, and 52, are directed to digital logic "configured ***with a single register write operation***" (emphasis added). The combination of Insenser and Furtek does not teach, suggest, or motivate the cited claim limitations of Independent Claims 11, 17, 35, 37, 42, 51, and 52. Therefore, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 are patentable over the combination of Insenser and Furtek and are in condition for allowance for reasons discussed in connection with Independent Claim 1.

Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are dependent on allowable Independent Claim 11, 17, 35, 37, 42, 51, and 52, which are allowable over the combination of Insenser and Furtek. Hence, it is respectfully submitted that Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are patentable over the combination of Insenser and Furtek for the reasons discussed above.

Claims 58-59 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Gamal et al., U.S. Patent No. 5,754,826 (hereafter Gamal). These rejections are respectfully traversed.

Independent Claim 58 recites (as amended):

> In a system disposed in an integrated circuit, said system comprising:
>
> a microcontroller comprising a non-volatile program memory;
>
> a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program memory, wherein each digital functionality ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***;
>
> an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and
>
> a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:
>
> a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions
>
> b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;
>
> c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and
>
> d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c). (emphasis added)

It is respectfully asserted that the combination of Insenser and Gamal does not teach, suggest, or motivate the present invention as recited in Independent Claim 58. In particular, the Independent Claim 58 recites the limitation, "each digital functionality ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a***

single register write operation," (emphasis added). In contrast, Insenser states that the FIPSOC architecture is reconfigurable by issuing a microprocessor command, and the reconfiguration time would be that of a microprocessor write cycle. [Insenser; Col. 5, lines 1-9]. However, Insenser fails to teach, suggest, or motivate that a dynamically configurable and programmable digital functional block is configurable with a single register write operation, as in the invention of Independent Claim 58. Further, Gamal fails to teach, suggest, or motivate that a dynamically configurable and programmable digital functional block is configurable with a single register write operation, as in the invention of Independent Claim 58.

As described above, the combination of Insenser and Gamal does not teach, suggest, or motivate the cited claim limitation of Independent Claim 58. Therefore, it is respectfully submitted that Independent Claim 58 is patentable over the combination of Insenser and Gamal and is in condition for allowance.

Dependent Claim 59 is dependent on allowable Independent Claim 58, which is allowable over the combination of Insenser and Gamal. Hence, it is respectfully submitted that Dependent Claim 59 is patentable over the combination of Insenser and Gamal for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above claims, arguments and remarks overcome all rejections and objections. All remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are in condition for allowance.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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Respectfully submitted,

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